CALL 2011-1

Project profile

ELESIS

European library-based flow of embedded silicon test instruments

Many of today's integrated circuits have reached such a high level of complexity that testing of individual components during production is reliant on equally complex and expensive automated test equipment. The ENIAC JU project ELESIS aims to define and standardise built-in chip test features with a common interface that will enable the identification of faults relatively inexpensively and thus reduce production costs. The primary target will be those containing analogue, radio frequency and sensor components as they are particularly difficult to isolate for an analysis of the test parameters.

Sub Programme

- Design methods and tools for nanotechnologies

Production testing of integrated circuits (ICs) is currently carried-out using large and expensive automatic test equipment. While chip production costs decrease with each new technology node, the cost of testing remains flat or increases, particularly for ICs with analogue, radio-frequency (RF) or sensor components. Test features integrated into the chip will take advantage of the silicon scaling that would translate into overall cost benefits, including testing costs.

Improving infrastructure

The ENIAC JU project ELESIS project is focusing on the development of built-in test functions to improve the industrial test infrastructure for ICs enabling European manufacturers to produce safe, reliable, high quality, low cost chips. The ambitious project plans to cover safety, reliability, high quality and low cost for mixed signal circuits in addition to digital circuits and memories, with special focus on analogue, RF and sensor components.

ELESIS is also targeting a European standard interface to reduce test complexity and to manage access to the internal circuit blocks. It will address the most significant aspects of semiconductor testing within a framework of embedded test instruments controlled through a common interface to ensure the best solutions to reach the challenging targets.

The proposed standard interface will have a large economic impact through the creation of an open-source platform which could be used by all chipmakers in Europe and even worldwide.

Built-in self test

Built-in self-test (BIST) as a concept is a well-known solution for digital logic and memories but it is in its infancy as far as analogue, RF and sensor components are concerned. Although such solutions do exist they are usually limited to one application. While this approach does reduce recurring test costs, it increases design and test development costs.

Moreover, it increases the time to market as a new test solution has to be developed for each design.

To really benefit from this self-test concept, generic BIST solutions which rely on standard embeddable testing resources are required. Furthermore, to ensure fast test integration and interoperability, these generic solutions need a common access and control interface.

Structurally-based built-in test (BIT) solutions greatly improve test efficiency and reduce cost but coverage in terms of defect detection and/or parameter observation is often inadequate. Ideally, both BIST and functional test solutions are required. A hardware test solution, driven by a BIT approach and improved with functional test capabilities, is called a 'test instrument'.

Embedded instruments

Another advantage of the BIT approach is that it allows for the testing of ICs in parallel, further reducing test costs. BIT also enables the checking of ICs during service and provides either an early warning or redundancy repair and thereby prevents a malfunction. Finally, embedded test instruments can also provide crucial information for facilitating failure diagnosis at any moment in the device life.

Reliability is one of the major challenges of mixed signal analogue circuits. Consequently, it is not sufficient to test a unit once after production – continuous monitoring is required during operation. Embedded test instruments provide that possibility.

ELESIS is promoting the development of a framework of embedded test instruments controlled through a common interface. Key characteristics are:

- A standardised common control interface;
- Efficient, low-cost test solutions close to generic for analogue and digital circuits;
- Development of new methodologies for yield and reliability analysis;
- Optimised capabilities regarding silicon area versus accuracy;
- Transparency with respect to the normal device function;
- Easily testable with low probability of failure due to the reduced area; and
- Methods for integration and industrialisation of the proposed solutions.

Comprehensive testing

European chipmakers will introduce many new devices in coming years. Typical applications will be found in road safety, personal health care, secure wireless communications, lighting and consumer electronics. These applications concern very complex systems with highly-integrated technologies where digital, memory and analogue circuits are embedded in one piece of silicon.

Reliability and durability cannot be guaranteed without extensive and comprehensive testing. ELESIS involves co-operation between leading chipmakers, small and medium-sized enterprises dedicated to systems testing and tooling, and respected European institutes and universities .The successful completion of this project will put European semiconductor manufacturers at the forefront of the silicon industry worldwide.

Design methods and tools

Partners:
- ATMEL
- CEA
- CNRS-LIRMM
- D4T Systems
- INESC Porto
- Infineon Technologies
- IPG/TIMA
- iRoC Technologies
- JTAG Technologies
- NXP Semiconductors
- NXP Semiconductors France
- PRESTO Engineering
- Salland Engineering
- STMicroelectronics
- Temento Systems
- University of Twente

Project co-ordinator:
- Mohamed Azimane, NXP Semiconductors

Key project dates:
- Start: June 2012
- Finish: June 2015

Countries involved:
- Austria
- France
- The Netherlands
- Portugal

Total budget:
- €23.98 million

The ENIAC Joint Undertaking, set up in February 2008, co-ordinates European nanoelectronics research activities through competitive calls for proposals. It takes public-private partnerships to the next level, bringing together the ENIAC member states, the European Commission and AENEAS, the association of R&D actors in this field, to foster growth and reinforce sustainable European competitiveness.

Details correct at time of print but subject to possible change. Updates will be included in the project summary at the end of the project.

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