European Library of Embedded Silicon Test Instruments

IP DATA SHEET *Sigma-Delta ADC BIST*

FEATURES

- Full-BIST dynamic characterization of Sigma-Delta ADCs.
- Measurement of SNDR of the converter.
- The BIST IP can be adapted to any discrete-time sigma-delta modulator implementation.
- Test stimulus injection requires the modification of the input integrator in the modulator (addition of input switches).
- Both amplitude and frequency of the test stimulus can be designed and programmed to cope with specific test needs.

TEST INTERFACE

- Standard SPI protocol

IO REQUIREMENTS

- INPUTS
  - o SPI serial input signals (SDI, CK, CS)
- OUTPUTS
  - o SPI serial output signal (SDO)

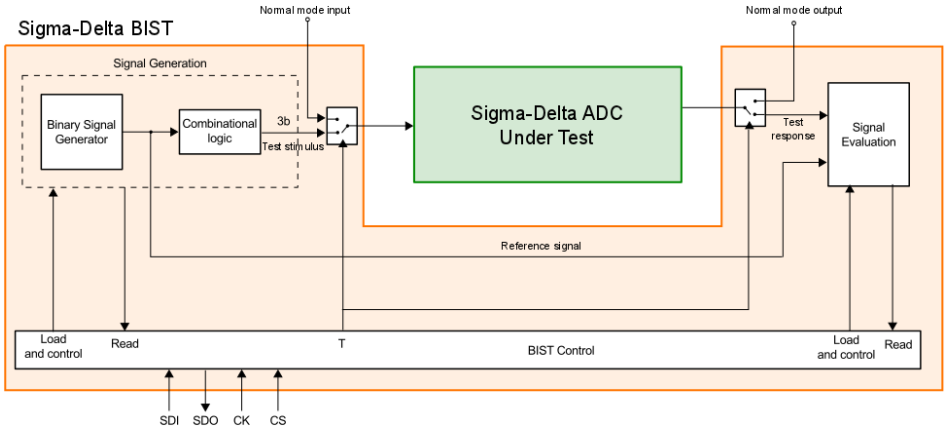
PARAMETERS

- INPUTS
  - o Optimized Sigma-Delta stimulus
  - o Test reference values
- OUTPUTS
  - o SNDR estimation
  - o Go/No-Go flag

OVERVIEW

This test instrument is aimed at the on-chip characterization of the dynamic performance of discrete-time Sigma-Delta ADCs. The proposed BIST IP includes an innovative ternary test stimulus generator that allows an accurate estimation of the SNDR of the converter at input amplitudes very close to the FS range. Signal analysis is performed using a simplified version of the sine-wave fitting algorithm, and the functionality of the complete IP can be managed through a standard SPI controller.

DESCRIPTION OF THE IP ARCHITECTURE



The proposed BIST architecture features a simple modification of the input of the analog modulators for injecting the digital test stimulus and a digital BIST wrapper. The digital wrapper includes stimulus generation, response analysis, and BIST control.

The IP is composed of the following modules:

➢ **MODULE 1: Stimulus generation**

The stimulus generation module is composed of two main blocks: a digital circular shift-register which must be loaded with an optimized sigma-delta bit-stream that encodes a sinusoidal test signal, and some combination logic that builds the ternary test stimulus by adding the binary bit-stream in the shift-register to a delayed version of the same signal.

➢ **MODULE 2: Signal Evaluation**

The signal evaluation module implements a simplified version of the sine-wave-fitting algorithm to compute the SNDR of the ADC under test by comparing the test response to an in-phase reference signal.

➢ **MODULE 3: BIST control**

The BIST control module selects the ADC to be tested, controls both stimulus generation and response analysis during test, and provides a standard interface based using the SPI protocol for loading test data and reading test results.

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DELIVERABLES

- Optimization software for automatic generation of high-spectral purity sigma-delta bit-streams.

LIMITATIONS

- Fixed precision of the SNDR estimation. Precision depends on the number of samples of the test response taken for evaluation.
- Fixed test frequency due to the fixed length of shift-register in the stimulus generation module. Nevertheless, the test frequency encoded in the IP can be parameterized at VHDL design level.
- The analysis algorithm does not separate noise from distortion. The measurement of SNR is not possible.

IP CONTROL INSTRUCTIONS

- Test mode/Normal mode switch
- Writing instructions (test mode): Loading of test configuration. Main commands include:
  - ❖ Load test stimulus: writes an optimized binary test sequence to the stimulus generation module.
  - ❖ Load Threshold: writes a comparison threshold for the SNDR to the signal evaluation module. This threshold is used to trigger the Go/No-Go flag.
  - ❖ Load Reference: writes the amplitude of the reference signal into the signal evaluation module. This value is used in the sine-wave fitting algorithm.
- Reading instructions (test mode): Reading out of test results and selected internal test registers (on demand). Main commands include:
  - ❖ Read Error Power: reads out the combined noise plus distortion power computed by the signal evaluation module from the test response signal.
  - ❖ Read Go/No-Go: reads out the binary value of the Go/No-Go flag computed by the signal evaluation module. This value is high if the SNDR of the test response is above a predefined threshold and low otherwise.
  - ❖ Read Amplitude and DC: reads out the amplitude and DC level of the test response signal computed by the signal evaluation module
  - ❖ Read Test Stimulus: reads out the optimized test sequence previously loaded in the signal generation module for diagnosis purposes.

IP TEST MESSAGES

- Go/No-Go flag
- SNDR estimation

VALIDATION RESULTS

The Sigma-Delta BIST IP has been validated on an 18-bit stereo sigma-delta ADC for audio applications provided by STMicroelectronics. Mixed-signal simulation results show the feasibility of the developed prototype. The measurement of the converter SNDR have been demonstrated up to -4dBFS for a 5 KHz stimulus, achieving less than 1dB deviation with respect to the traditional functional measurements. Additionally, the introduction of the BIST has been proved to have no significant impact to the converter performance. An integrated demonstrator has been sent for fabrication in a CMOS 40nm technology to further validate the proposed test instrument.

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